AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-3. (canceled).

4. (currently amended): A liquid crystal display device driving method wherein said liquid crystal display device comprises:~~The liquid crystal display device driving method according to claim 3,~~

a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines;

a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period;

a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period;

a matrix substrate on which said data driver circuit and said gate driver circuit are formed;

a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode common to all said pixels on said matrix substrate is arranged,

wherein said data driver circuit comprises N switching blocks each having M switching elements, a scanning circuit for outputting an open/close control signal for each switching block, and M x P (P is a natural number) video signal wirings forming one set of M x N video signals from said video signal corresponding to a first pixel time period up to said video signal corresponding to a final pixel time period within the horizontal time period as one set; said M video signal wirings of an i-th set (one of i = 1, 2, ..., P) of the M x P video signal wirings are respectively connected to input terminals of the M switching elements of the i-th switching block, when viewed from the first switching block, and

wherein said data lines are divided into blocks each having M data lines, wherein said M data lines of each block are respectively connected to output terminals of said M switching elements within each of the switching blocks from a first switching block up to a final switching block of the N switching blocks defined in blocks from a first block up to a final block, said driving method comprising:

an outputting step wherein said scanning circuit outputs the open/close control signal synchronously with the M video signals supplied successively every P sets, and successively outputs every set of the P sets simultaneously within the set through the M x P video signal wirings in an arbitrary horizontal time period;

a sampling step wherein the M video signals, which are supplied successively every P sets, successively every set of the P sets and simultaneously within the set, are sampled to the M data lines connected to the M switching elements so as to simultaneously conduct in the M switching elements of the switching block,

wherein at a time instant when a first time period of a conduction time period when each of the M switching elements is in the conducting state elapses from a time instant of start of the conduction of the M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit, the open/close control signal is supplied from the scanning circuit to the switching block in which the M switching elements simultaneously conduct subsequent to M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit; and

a writing step wherein the M video signals that are sampled individually are respectively written to the M pixels of the set including the M pixel transistors, and are caused to simultaneously conduct through the M pixel transistors of the set every set of M pixel transistors which are connected to the gate lines through which the gate driver circuit supplies the gate signal during the arbitrary horizontal time period and which simultaneously conduct,

wherein the M video signals supplied through the M video signal wirings for each set of the P sets are the video signals the polarity of which is changed with respect to the counter electrode between the first time period and a second time period as the remaining time period of the conduction time period following the first time period.

5-7. (canceled).

8. (currently amended): A liquid crystal display device driving method wherein said liquid crystal display device comprises:~~The liquid crystal display device driving method according to claim 7,~~

a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines;

a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period;

a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period;

a matrix substrate on which said data driver circuit and said gate driver circuit are formed,

a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode common to all said pixels on said matrix substrate is arranged;

wherein said data driver circuit comprises N switching block each having M switching elements, a scanning circuit for outputting an open/close control signal for each switching block, and 2M video signal wirings forming one set of said 2M video signals from said video signal corresponding to a first pixel time period up to said video signal corresponding to a final pixel time period within the horizontal time period as one set; said M video signal wirings of an i-th set (one of i = 1, 2, ..., P) of the 2M video signal wirings are respectively connected to input terminals of the M switching elements of the i-th switching block; and

wherein said data lines are divided into blocks each having said M data lines, wherein said M data lines of each block are respectively connected to output terminals of said M switching elements within each of the switching blocks from a first switching block up to a final switching block of the N switching blocks defined in blocks from a first block up to a final block, said driving method comprising:

an outputting step wherein said scanning circuit outputs the open/close control signal synchronously with the M video signals supplied successively every P sets, and successively outputs every set of the P sets simultaneously within the set through the 2M video signal wirings in an arbitrary horizontal time period,

a sampling step wherein the M video signals, which are supplied successively every P sets, successively every set of the two sets and simultaneously within the set, are sampled to the M data lines connected to the M switching elements so as to simultaneously conduct in the M switching elements of the switching block; and

a writing step wherein the M video signals that are sampled individually are respectively written to the M pixels of the set including the M pixel transistors, and are caused to simultaneously conduct through the M pixel transistors of the set every set of M pixel transistors which are connected to the gate lines through which the gate driver circuit supplies the gate signal during the arbitrary horizontal time period and which simultaneously conduct,

wherein at a time instant when a first time period of a conduction time period when each of the M switching elements is in the conducting state elapses from a time instant of start of the conduction of the M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit, the

open/close control signal is supplied from the scanning circuit to the switching block in which the M switching elements simultaneously conduct subsequent to M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit, and

wherein the M video signals supplied through the M video signal wirings for each set of the P sets are the video signals the polarity of which is changed with respect to the counter electrode between the first time period and a second time period as the remaining time period of the conduction time period following the first time period.

9. (original): The method of driving a liquid crystal display device according to claim 4, characterized in that a time instant when the polarity of each video signal changes between the first time period and the second time period is a time instant which precedes a time instant when the switching elements of the switch block transition from the conducting state to the nonconducting state in a predetermined time period.

10. (original): The method of driving a liquid crystal display device according to claim 8, characterized in that a time instant when the polarity of each video signal changes between the first time period and the second time period is a time instant which precedes a time instant when the switching elements of the switch block transition from the conducting state to the nonconducting state in a predetermined time period.

11. (original): The method of driving a liquid crystal display device according to claim 4, characterized in that the ratio of the first time period to the second time period is a predetermined ratio which acts to reduce in quantity of voltage fluctuations of the video signals on all of the data lines.

12. (original): The method of driving a liquid crystal display device according to claim 8, characterized in that the ratio of the first time period to the second time period is a predetermined ratio which acts to reduce in quantity of voltage fluctuations of the video signals on all of the data lines.

13. (original): The method of driving a liquid crystal display device according to claim 4, characterized in that the first time period is a time period which is equal to or shorter than the first half of the conduction time period, and the second time period is the remaining time period just following the time period which is equal to or shorter than the first half thereof.

14. (original): The method of driving a liquid crystal display device according to claim 8, characterized in that the first time period is a time period which is equal to or shorter than the first half of the conduction time period, and the second time period is the remaining time period just following the time period which is equal to or shorter than the first half thereof.

15-18. (canceled).

19. (currently amended): A liquid crystal display device comprising: ~~The liquid crystal display device according to claim 18,~~

a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines:

a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period;

a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period;

a matrix substrate on which said data driver circuit and said gate driver circuit are formed; and

a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode common to all said pixels on said matrix substrate is arranged,

wherein said data driver circuit comprises by N switching blocks each having M switching elements, a scanning circuit for outputting an open/close control signal for each switching block, and M x P (P is a natural number) video signal wirings forming one set of said M x N video signals from said video signal corresponding to a first pixel time period up to said video signal corresponding to a final pixel time period within the horizontal time period as one set, said M video signal wirings of an i-th set (one of i = 1, 2, ..., P) of the M x P video signal wirings are respectively connected to input terminals of the M switching elements of the i-th switching block,

wherein said data lines are divided into blocks each having M data lines, wherein said M data lines of each block are respectively connected to output terminals of said M switching elements within each of the switching blocks from a first switching block up to a final switching block of the N switching blocks defined in blocks from a first block up to a final block,

wherein the scanning circuit outputs the open/close control signal synchronously with the M video signals supplied successively every P sets, and successively outputs every set of the P sets simultaneously within the set through the M x P video signal wirings in an arbitrary horizontal time period,

wherein the M video signals, which are supplied successively every P sets, successively every set of the P sets and simultaneously within the set, are sampled to the M data lines connected to the M switching elements which simultaneously conduct in the M switching elements of the switching block,

wherein at a time instant when a first time period of a conduction time period when each of the M switching elements is in the conducting state elapses from a time instant of start of the conduction of the M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit, the open/close control signal is supplied from the scanning circuit to the switching block in which the M switching elements simultaneously conduct on the heels of M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit,

wherein the M video signals that are sampled individually are respectively written to the M pixels of the set including the M pixel transistors which simultaneously conduct through the

M pixel transistors of the set every set of M pixel transistors which are connected to the gate lines through which the gate driver circuit supplies the gate signal during the arbitrary horizontal time period and which simultaneously conduct, and

wherein the M video signals supplied through the M video signal wirings for each set of the P sets are the video signals the polarity of which is changed with respect to the counter electrode between the first time period and a second time period as the remaining time period of the conduction time period following the first time period.

20-22. (canceled).

23. (original): A liquid crystal display device comprising:~~The liquid crystal display device according to claim 22,~~

a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines;

a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period;

a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period;

a matrix substrate on which said data driver circuit and said gate driver circuit are formed; and

a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode common to all said pixels on said matrix substrate is arranged,

wherein said data driver circuit comprises by N switching block each having M switching elements, a scanning circuit for outputting an open/close control signal for each switching block, and 2M video signal wirings forming one set of said M x N video signals from said video signal corresponding to a first pixel time period up to said video signal corresponding to a final pixel time period within the horizontal time period as one set; said M video signal wirings of an i-th set (one of i = 1, 2, ..., P) of the 2M video signal wirings are respectively connected to input terminals of the M switching elements of the i-th switching block,

wherein said data lines are divided into blocks each having said M data lines, wherein said M data lines of each block are respectively connected to output terminals of said M switching elements within each of the switching blocks from a first switching block up to a final switching block of the N switching blocks defined in blocks from a first block up to a final block,

wherein the scanning circuit outputs the open/close control signal synchronously with the M video signals supplied successively every two sets, and successively outputs every set of the two sets simultaneously within the set through the 2M video signal wirings in an arbitrary horizontal time period,

wherein the M video signals, which are supplied successively every two sets, successively every set of the two sets and simultaneously within the set, arc sampled to the M data lines connected to the M switching elements which are caused to simultaneously conduct in the M switching elements of the switching block,

wherein the M video signals that are sampled individually are respectively written to the M pixels of the set including the M pixel transistors which simultaneously conduct through the M pixel transistors of the set every set of M pixel transistors which are connected to the gate lines through which the gate driver circuit supplies the gate signal during, the arbitrary horizontal time period and which simultaneously conduct,

wherein at a time instant when a first time period of a conduction time period when each of the M switching elements is in the conducting state elapses from a time instant of start of the conduction of the M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit, the open/close control signal is supplied from the scanning circuit to the switching block in which the M switching elements simultaneously conduct subsequent to M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit,; and

wherein the M video signals supplied through the M video signal wirings for each set of the P sets are the video signals the polarity of which is changed with respect to the counter electrode between the first time period and a second time period as the remaining time period of the conduction time period following the first time period.

24. (original): The liquid crystal display device according to claim 19, characterized in that a time instant when the polarity of each video signal changes between the first time period and the second time period, is a time instant which precedes a time instant when the switching elements of the switch block transition from the conducting state to the nonconducting state in a predetermined

time period.

25. (original): The liquid crystal display device according to claim 23, characterized in that a time instant when the polarity of each video signal changes between the first time period and the second time period is a time instant which precedes a time instant when the switching elements of the switch block transition from the conducting state to the nonconducting state in a predetermined time period.

26. (original): The liquid crystal display device according to claim 19, characterized in that the ratio of the first time period to the second time period is a predetermined ratio which acts to reduce in quantity of voltage fluctuations of the video signals on all the data lines.

27. (original): The liquid crystal display device according to claim 23, characterized in that the ratio of the first time period to the second time period is a predetermined ratio which acts to reduce in quantity of voltage fluctuations of the video signals on all the data lines.

28. (original): The liquid crystal display device according to claim 19, characterized in that the first time period is a time period which is equal to or shorter than the first half of the conduction time period, and the second time period is the remaining time period just following the time period which is equal to or shorter than the first half thereof.

29. (original): The liquid crystal display device according to claim 23, characterized in that

the first time period is the time period which is equal to or shorter than the first half of the conduction time period, and the second time period is the remaining time period just following the time period which is equal to or shorter than the first half thereof.

30. (original): The liquid crystal display device according to claim 19, characterized in that the polarities of the video signals which are written to all the pixels are made either the same polarity with respect to the counter electrode or the opposite polarity with respect to the counter electrode for the preceding frame time period of the two preceding and following frame time periods when the video signals for one screen are successively displayed, wherein the polarities of the video signals which are written to all the pixels are made either the opposite polarity the polarity which is taken for the preceding time period or the same polarity for the following time period.

31. (original): The liquid crystal display device according to claim 23, characterized in that the polarities of the video signals which are written to all the pixels are made either the same polarity with respect to the counter electrode or the opposite polarity with respect to the counter electrode for the preceding frame time period of the two preceding and following frame time periods when the video signals for one screen are successively displayed, wherein the polarities of the video signals which are written to all the pixels are made either the opposite polarity from the polarity which is taken for the preceding time period or the same polarity for the following time period.

32. (original): The liquid crystal display device according to claim 19, characterized in that a P x Q or two video signal wirings are adapted to supply therethrough the video signals for one screen at a second frame frequency at least two times as high as a first frame frequency of a signal source for outputting the video signals for one picture at the first frame frequency so that the video signals are written to all the pixels two or more times.

33. (original): The liquid crystal display device according to claim 23, characterized in that a P x Q or two video signal wirings are adapted to supply therethrough the video signals for one screen at a second frame frequency at least two times as high as a first frame frequency of a signal source for outputting the video signals for one picture at the first frame frequency so that the video signals are written to all the pixels two or more times.

34. (original): The liquid crystal display device according to claim 19, characterized in that a TFT constituting the pixel switching element, and TFTs constituting the data driver circuit and the gate driver circuit comprise of polysilicon TFTs.

35. (original): The liquid crystal projector apparatus comprising the liquid crystal display device according to claim 19.

36. (original): A liquid crystal display device driving method, wherein said liquid crystal display device comprises:

a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said

gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines;

a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period;

a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period;

a matrix substrate on which said data driver circuit and said gate driver circuit are formed;

a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode common to all said pixels on said matrix substrate is arranged;

wherein said data driver circuit is comprised by video signal wirings through which the video signals from the video signal corresponding to the first time period up to the video signal corresponding to the final time period are adapted to be supplied every horizontal time period;

switching elements for connecting the video signal wirings to the data lines to which the video signals are to be respectively supplied; and a scanning circuit for outputting an open/close control signal in accordance with which the switching elements are caused to conduct,

the open/close control signal being supplied from the scanning circuit to the switching elements to which the video signals are supplied synchronously with the video signals supplied through the video signal wirings, respectively, said driving method comprising:

a step of supplying wherein the video signals supplied through the video signal wirings being sampled to the data lines to which the video signals are to be supplied in the switching elements which are caused to conduct with the open/close control signal, and

a step of sampling wherein the sampled video signals being passed through the pixel transistors which are connected to the gate line through which the gate signal is adapted to be supplied by the gate driver circuit and which are caused to conduct to be written to the pixels including the pixel transistors, respectively, for a supply horizontal period when the video signals are supplied to the video signal wirings, respectively,

wherein the video signals which are to be supplied to the video signal wirings to which the switching elements caused to conduct in accordance with the open/close control signal are connected are the video signals the polarity of which is changed with respect to the counter electrode between the first time period, which is in a conduction time period when the switching elements are caused to conduct with the open/close control signal, and a second time period as the remaining time period of the conduction time period following the first time period.

37. (original): A liquid crystal display device driving method, wherein said liquid crystal display device comprises:

a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines;

a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period;

a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period;

a matrix substrate on which said data driver circuit and said gate driver circuit are formed;

a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode common to all said pixels on said matrix substrate is arranged;

wherein said data driver circuit is comprised by video signal wirings through which the video signals from the video signal corresponding to the first time period up to the video signal corresponding to the final time period are adapted to be supplied every horizontal time period;

switching elements for connecting the video signal wirings to the data lines to which the video signals are to be respectively supplied; and a scanning circuit for outputting an open/close control signal in accordance with which the switching elements are caused to conduct,

the open/close control signal being supplied from the scanning circuit to the switching elements to which the video signals are supplied synchronously with the video signals supplied through the video signal wirings, respectively, said driving method comprising:

a step of supplying wherein the video signals supplied through the video signal wirings being sampled to the data lines to which the video signals are to be supplied in the switching elements which are caused to conduct with the open/close control signal, and

a step of sampling wherein the sampled video signals being passed through the pixel transistors which are connected to the gate line through which the gate signal is adapted to be supplied by the gate driver circuit and which are caused to conduct to be written to the pixels including the pixel transistors, respectively, for a supply horizontal period when the video signals are supplied to the video signal wirings, respectively,

wherein at a time instant when a first time period of a conduction time period when the

switching elements are in the conducting state elapses from a time instant of start of the conduction of the switching elements which are caused to conduct with the open/close control signal supplied from the scanning circuit, the open/close control signal is supplied from the scanning circuit to the switching elements which are to be caused to conduct on the heels of the switching elements which are caused to conduct in accordance with the open/close control signal supplied from the scanning circuit; and

the video signals which are to be supplied to the video signal wirings to which the switching elements caused to conduct in accordance with the open/close control signal supplied from the scanning circuit are connected are the video signals the polarity of which is changed with respect to the counter electrode between the first time period and a second time period as the remaining time period of the conduction time period following the first time period.

38. (original): The method of driving a liquid crystal display device according to claim 36, characterized in that a time instant when the polarity of each video signal changes between the first time period and the second time period, is a time instant which precedes a time instant when the switching elements of the switch block transition from the conducting state to the nonconducting state in a predetermined time period.

39. (original): The method of driving a liquid crystal display device according to claim 37, characterized in that a time instant when the polarity of each video signal changes between the first time period and the second time period, is a time instant which precedes a time instant when the switching elements of the switch block transition from the conducting state to the nonconducting

state in a predetermined time period.

40. (original): The method of driving a liquid crystal display device according to claim 36, characterized in that the ratio of the first time period to the second time period is a predetermined ratio which acts to reduce voltage fluctuations of the video signals.

41. (original): The method of driving a liquid crystal display device according to claim 37, characterized in that the ratio of the first time period to the second time period is a predetermined ratio which acts to reduce voltage fluctuations of the video signals.

42. (original): The method of driving a liquid crystal display device according to claim 36, characterized in that the first time period is the time period which is equal to or shorter than the first half of the conduction time period, and the second time period is the remaining time period just following the time period which is equal to or shorter than the first half thereof.

43. (original): The method of driving a liquid crystal display device according to claim 37, characterized in that the first time period is the time period which is equal to or shorter than the first half of the conduction time period, and the second time period is the remaining time period just following the time period which is equal to or shorter than the first half thereof.

44. (original): A liquid crystal display device comprising:

a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said

gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines;

a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period;

a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period;

a matrix substrate on which said data driver circuit and said gate driver circuit are formed;

a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode common to all said pixels on said matrix substrate is arranged;

wherein said data driver circuit comprises by video signal wirings through which the video signals from the video signal corresponding to the first time period up to the video signal corresponding to the final time period are adapted to be supplied every horizontal time period;

switching elements for connecting the video signal wirings to the data lines to which the video signals are to be respectively supplied; and a scanning circuit for outputting an open/close control signal in accordance with which the switching elements are caused to conduct,

the open/close control signal being supplied from the scanning circuit to the switching elements to which the video signals are supplied synchronously with the video signals supplied through the video signal wirings, respectively, the video signals supplied through the video signal wirings being sampled to the data lines to which the video signals are to be supplied in the switching elements which are caused to conduct with the open/close control signal, and

the sampled video signals being passed through the pixel transistors which are connected to

the gate line through which the gate signal is adapted to be supplied by the gate driver circuit and which are caused to conduct to be written to the pixels including the pixel transistors, respectively, for a supply horizontal period when the video signals are supplied to the video signal wirings, respectively,

wherein the video signals which are to be supplied to the video signal wirings to which the switching elements caused to conduct in accordance with the open/close control signal are connected are the video signals the polarity of which is changed with respect to the counter electrode between the first time period, which is in a conduction time period when the switching elements are caused to conduct with the open/close control signal, and a second time period as the remaining time period of the conduction time period following the first time period.

45. (original): A liquid crystal display device comprising:

a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines;

a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period;

a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period;

a matrix substrate on which said data driver circuit and said gate driver circuit *are* formed;

a liquid crystal sandwiched between said matrix substrate and a counter substrate on

which a counter electrode common to all said pixels on said matrix substrate is arranged;

wherein said data driver circuit comprises by video signal wirings through which the video signals from the video signal corresponding to the first time period up to the video signal corresponding to the final time period are adapted to be supplied every horizontal time period; switching elements for connecting the video signal wirings to the data lines to which the video signals are to be respectively supplied; and a scanning circuit for outputting an open/close control signal in accordance with which the switching elements are caused to conduct,

the open/close control signal being supplied from the scanning circuit to the switching elements to which the video signals are supplied synchronously with the video signals supplied through the video signal wirings, respectively,

the video signals supplied through the video signal wirings being sampled to the data lines to which the video signals are to be supplied in the switching elements which are caused to conduct with the open/close control signal, and

the sampled video signals being passed through the pixel transistors which are connected to the gate line through which the gate signal is adapted to be supplied by the gate driver circuit and which are caused to conduct to be written to the pixels including the pixel transistors, respectively, for a supply horizontal period when the video signals are supplied to the video signal wirings, respectively,

wherein at a time instant when a first time period of a conduction time period when the switching elements are in the conducting state elapses from a time instant of start of the conduction of the switching elements which are caused to conduct with the open/close control signal supplied from the scanning circuit, the open/close control signal is supplied from the

scanning circuit to the switching elements which are to be caused to conduct on the heels of the switching elements which are caused to conduct in accordance with the open/close control signal supplied from the scanning circuit; and

the video signals which are to be supplied to the video signal wirings to which the switching elements caused to conduct in accordance with the open/close control signal supplied from the scanning circuit are connected are the video signals the polarity of which is changed with respect to the counter electrode between the first time period and a second time period as the remaining time period of the conduction time period following the first time period.

46. (original): The liquid crystal display device according to claim 44, characterized in that a time instant when the polarity of each video signal changes between the first time period and the second time period, is a time instant which precedes a time instant when the switching elements of the switch block transition from the conducting state to the nonconducting state in a predetermined time period.

47. (original): The liquid crystal display device according to claim 45, characterized in that a time instant when the polarity of each video signal changes between the first time period and the second time period, is a time instant which precedes a time instant when the switching elements of the switch block transition from the conducting state to the nonconducting state in a predetermined time period.

48. (original): The liquid crystal display device according to claim 44, characterized in that

the ratio of the first time period to the second time period is a predetermined ratio which acts to reduce voltage fluctuations of the video signals.

49. (original): The liquid crystal display device according to claim 45, characterized in that the ratio of the first time period to the second time period is a predetermined ratio which acts to reduce voltage fluctuations of the video signals.

50. (original): The liquid crystal display device according to claim 44, characterized in that the first time period is the time period which is equal to or shorter than the first half of the conduction time period, and the second time period is the remaining time period just following the time period which is equal to or shorter than the first half thereof.

51. (original): The liquid crystal display device according to claim 45, characterized in that the first time period is the time period which is equal to or shorter than the first half of the conduction time period, and the second time period is the remaining time period just following the time period which is equal to or shorter than the first half thereof.